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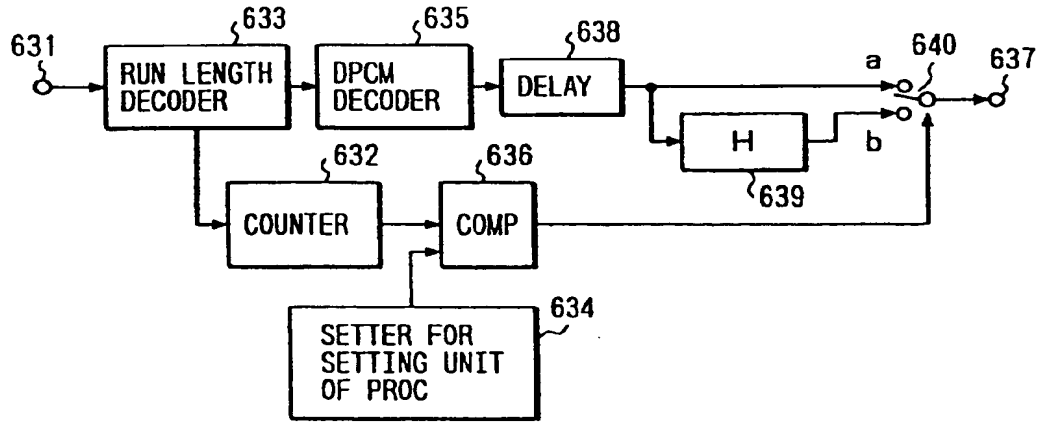
(54) Image processing apparatus

(57) An image processing apparatus and method in which an image signal including run-length encoded orthogonal transform coefficients is decoded and transmission errors in the coefficients are concealed by outputting substitute pixel data. Transmission errors are detected by counting the number of orthogonal transform coefficients, inclusive of those of 0-value included in each run, for a predetermined number of pixel block or blocks and by comparing the count obtained with a preset count.

FIG. 12



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an image processing apparatus, and more particularly to an image processing apparatus equipped with image decoding means which has a function of expanding compressed image data, for example.

Related Background Art

Conventionally, there is known a technique for transmitting image data after performing a frequency transform (transformation) of image data for each block to make data compression. In particular, by separating frequency components into a high-frequency component and a low-frequency component and encoding those components separately from each other, compression efficiency of images is increased.

However, the above prior art has had a disadvantage that if an error occurs during transmission of encoded data, an image signal including false image data is reproduced and image quality deteriorates remarkably. In the case of using a variable-length code in encoding the above high-frequency component, it may sometimes happen that even the number of data is not reproduced accurately and a quite gross deterioration of image quality such as missing of image data occurs.

Meanwhile, in the field of transmitting images in the digital form, there have also conventionally been proposed a variety of encoding methods for cutting down the quantity of information before transmitting images because the quantity of information is very large.

Among them, there is known a method of carrying out an orthogonal transform, quantizing a coefficient after the transform, and forming a variable-length code.

With the above-mentioned prior art including no error detecting means, however, if an error occurs in a transmission path, such an error cannot be corrected, leading to a gross deterioration of image quality.

Especially, in the event of exceeding a dynamic range capable of decoding and reproducing when encoded data after transmission is decoded, for example, image quality deteriorates.

Moreover, in an image transmission system of the type that a moving image signal is digitized and image data is transmitted via transmission paths such as optical fibers or communication satellites and recording media such as magnetic tapes, an error correcting code (ECC) for detecting and correcting a transmission error is utilized to correct the transmission error in the reception side (or the reproduction side) based on the error correcting code. That error which cannot be corrected by using the error correcting code is subjected to interpolation processing to form an approximate value from surrounding pixels.

In order to avoid a deterioration of image quality caused by the interpolation processing, it is required that the surrounding pixels utilized for the interpolation are free from errors. When adopting highly efficient encoding (image compression) which has been widely used in recent years, the surrounding pixels capable of being utilized for the interpolation are restricted. In a DPCM (difference pulse code modulation) method that reset is made for each line, for example, if an uncorrectable error occurs, the original data cannot be reproduced by using the line inclusive of the error. Accordingly, only those pixels which are included in the upper and lower lines can be utilized for interpolation in this case. Further, in an encoding method that uses an orthogonal transform such as a discrete cosine transform (DCT), if an uncorrectable error occurs, all the pixels included in a transmission block (e.g., 8 pixels vertical x 8 pixels horizontal) cannot be used to reproduce the original signal. As a result, a deterioration of image quality cannot be prevented even by the interpolation using the upper and lower lines.

Thus, even in an attempt of performing the interpolation in the same frame, no effect may be expected depending on the coding methods.

Additionally, in the field of transmitting information such as images and voices in the digital form, there have been proposed various encoding methods for cutting down the amount of data transmitted. One known run-length coding method is to encode data by combining the number of successive 0s and a value other than 0 into a set. On the other hand, a forecast difference encoding method or a difference pulse code modulation (hereinafter referred to as DPCM) encoding method is also known which compresses information by utilizing correlation between sample values close to each other. There is further known an encoding method that the above two methods are combined with each other. Fig. 14 is a block diagram showing the encoding method in a combination of the two methods. Image data of 8 bits inputted through an input terminal 611 is applied to a DPCM encoder 613 for DPCM encoding into 4 bits. Specifically, the DPCM encoder 613 assigns DPCM codes of 4 bits to respective difference values as shown in Table 1 below.

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Table 1

Range of Difference Values	DPCM Code	Representative Value of Difference
- 255 ~ - 94	15	- 140
- 93 ~ - 70	13	- 80
- 69 ~ - 50	11	- 58
- 49 ~ - 34	9	- 40
- 33 ~ - 22	7	- 27
- 21 ~ - 13	5	- 17
- 12 ~ - 6	3	- 8
- 5 ~ - 2	1	- 3
- 1 ~ 1	0	0
2 ~ 5	2	3
6 ~ 11	4	8
12 ~ 20	6	15
21 ~ 35	8	27
36 ~ 53	10	44
54 ~ 93	12	70
94 ~ 255	14	150

An image generally has correlation between sample values close to each other such that many difference signals occur as 0 and many DPCM codes occur as 0. The DPCM codes encoded into 4 bits are outputted to a run-length encoder 615. As shown in Fig. 15A, the run-length encoder 615 combines the DPCM code other than 0 and the number of successive 0s (hereinafter referred to as a 0 run-length) before the DPCM code into a set for each DPCM code of 4 bits.

At this time, by limiting the 0 run-length to 16 at maximum, the run-length codes can be each expressed in 8 bits. The 8-bit run-length codes thus encoded by the run-length encoder 615 are added with a reset synch bit in a transmission format unit 617 as shown in Fig. 15B and then delivered to an output terminal. The reset synch bit is added, for example, after processing of each line.

Fig. 13 is a block diagram showing a configuration of a decoder device in cooperation with the encoding section of Fig. 14. The run-length code and the reset synch bit both transmitted through a transmission path are applied to an input terminal 621, and a run-length decoder 623 decodes the DPCM code by inserting 0s in the number corresponding to the 0 run-length before each DPCM code until arrival of the reset synch bit. The data decoded to the DPCM code is outputted to a DPCM decoder 625 for decoding to image data of 8 bits, which are then delivered to an output terminal 627.

With the above conventional method, however, if an error occurs in a transmission path, such an error cannot be corrected and image quality deteriorates remarkably because of including no error detecting means.

As mentioned before, in the field of transmitting information such as images and voices in the digital form, there have been proposed various encoding methods for cutting down the amount of data transmitted. One known run-length coding method is to encode data by combining the number of successive 0s and a value other than 0 into a set. On the other hand, a transform encoding method is also known which performs an orthogonal transform of pixels to be transmitted and quantizes transmitted data. There is further known an encoding method that the above two methods are combined with each other.

With the above conventional methods, however, if an error occurs in a transmission path, such an error cannot be corrected and image quality deteriorates remarkably because of including no error detecting means.

Meanwhile, U.S. Patent No. 5,023,919 has been proposed with an intention to correct or avoid a deterioration on the side decoding compressed data, but has not yet succeeded in sufficiently solving the problem.

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SUMMARY OF THE INVENTION

The present invention has been made in view of the situations in the prior art as set forth above, and its object is to provide an image processing apparatus which can satisfactorily control the amount of compressed data.

To achieve the above object, in accordance with the present invention, there is disclosed an image processing apparatus comprising, receiving means for receiving encoded image data which is encoded by using orthogonal transform in a predetermined block unit, error detecting means for detecting a transmission error of the encoded image data, correcting means for correcting the transmission error in the predetermined block unit, and decoding means for decoding the encoded image data and outputting image data for reproducing an image.

Another object of the present invention is to output a moving picture of high quality.

To achieve the above object, in accordance with the present invention, there is disclosed a moving picture processing apparatus comprising receiving means for receiving a plurality of pictures of encoded image data sequentially which is encoded by using orthogonal transform in a predetermined block unit, error detecting means for detecting a transmission error of one of the plurality of pictures, correcting means for correcting the transmission error by using encoded image data of another picture, and decoding means for decoding the encoded image data and outputting a plurality of pictures of image data sequentially for reproducing an image.

Still another object of the present invention is to improve a decoding method of encoded data which in encoded by run-length encoding. To achieve the above object, in accordance with the present invention, there is disclosed an image processing apparatus comprising receiving means for receiving an encoded orthogonal transform coefficient which is encoded by using run-length encoding method, decoding means for decoding the encoded orthogonal transform coefficient, error detecting means for detecting a transmission error of the encoded orthogonal transform coefficient based on the orthogonal transform coefficient, and correcting means for correcting the transmission error of the decoded orthogonal transform coefficient.

Still another object of the present invention is to improve an encoding method. To achieve the above object, in accordance with the present invention, there is disclosed an image processing apparatus comprising input means for inputting image data, transforming means for performing an orthogonal transform on the input image data, extracting means for extracting DC component and AC component from the transformed image data, adding means for adding data for error detection to at least one of the DC component and the AC component, and encoding means for encoding the DC component and the AC component.

Other objects and forms of the present invention will be apparent from the following explanation with reference to the drawings and the description in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a configuration of a first embodiment of the present invention.
Fig. 2 is a diagram showing one example of a data transmission format.
Fig. 3 is a block diagram showing a configuration of a second embodiment of the present invention.
Fig. 4 is a block diagram showing a configuration of a third embodiment of the present invention.
Fig. 5 is a block diagram showing a configuration of a decoding device in a fourth embodiment of the present invention.
Fig. 6 is a block diagram showing an encoding device in the fourth embodiment.
Fig. 7 is a diagram for explaining a zig-zag scanner 57 in Fig. 5.
Fig. 8 is a diagram for explaining a scan recovery unit 21 in Fig. 5.
Fig. 9 is a block diagram showing a configuration of a fifth embodiment of the present invention.
Fig. 10 is a circuit diagram of each of correlation detecting circuits 230, 232.
Fig. 11 is a block diagram showing a configuration of a sixth embodiment of the present invention
Fig. 12 is a block diagram showing a configuration of a seventh embodiment of the present invention.
Fig. 13 is a block diagram of a conventional decoding device.
Fig. 14 is a block diagram of a conventional encoding device.
Figs. 15A and 15B are diagrams for explaining operation of Fig. 14.
Fig. 16 is a block diagram showing a configuration of an eighth embodiment of the present invention.
Fig. 17 is a block diagram of an encoding device.
Figs. 18A and 18B are diagrams for explaining operation of Fig. 17.
Figs. 19, 20 and 21 are diagrams for explaining operation of Fig. 17.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

(First Embodiment)

An image decoding device according to a first embodiment of the present invention, described below, is featured in comprising means for detecting and correcting an error caused during transmission or in reproduction from a recording medium, and means for replacing decoded data in the relevant block by a predetermined setting value based on error information produced from the detecting and correcting means. After detecting an error caused on a transmission path and carrying out correction processing, if it is found that the relevant block has a DC component free from an error and an AC component still including an uncorrectable error, all the data in the relevant block are replaced by a value of the DC component based on such information, so that each pixel value in the relevant block can be replaced by a value close to a true value.

Fig. 1 illustrates a block diagram showing a configuration of an image decoding device and a corresponding image encoding device of this embodiment.

Denoted at reference numeral 401 is an encoding device and 402 is a decoding device, both the devices being connected to each other via a transmission path 403. The transmission path 403 is in the form of a transmission medium for aboveground electric-wave or light space, such as an optical fibre, satellite or microwave guide, in the case of instantaneous transmission, and in the form of a storage medium including a tape-like medium such as a digital VTR or DAT, a disk-like medium such as a floppy disk or optical disk, and a solid state medium such as a semiconductor memory.

First, a video signal inputted from an image reader comprising CCD sensors, TV camera, video recorder, hostcomputer or the like is applied to an input terminal 404 of the encoding device 401 and divided in a block formation circuit 406 into blocks each of which comprises a plurality of data, e.g., blocks each consisting of 8 x 8 pixels. The data thus divided in units of block is transformed in an orthogonal transform circuit 407 into frequency components for each block by, for example, a DCT (discrete cosine transform). The transformed data is outputted as a low-frequency component and a high-frequency component, for example, a DC (direct current) component and an AC (alternating current) component other than the former, in separate fashion. These components are separately encoded by encoding circuits 408, 409 for compressing the amount of information. As examples of the encoding, the DC component may be encoded by a PCM (pulse code modulation) encoding method and the AC component may be encoded by a run-length Huffman encoding method. Respective encoded data outputted from the encoding circuits 408,409 are further encoded by Error Correction Code (ECC) encoding circuits 410, 411 to have error detecting and correcting codes as a measure for coping with an error possibly caused during transmission, and then synthesized by a synthesis circuit 412 together in a time-serial manner. After that, the synthesized data is added in a synch signal addition circuit 413 with a synch signal for each predetermined number of blocks for the purpose of transmission or recording, followed by delivery into the transmission path 403.

Meanwhile, as for the data transmitted and received by the image decoding device 402, the synch signal is detected by a synch signal detecting circuit 101 and the following signal processing is carried out on the basis of the detected synch signal.

The transmitted data is first separated by a separation circuit 102 into encoded data corresponding to the DC component and encoded data corresponding to the AC component. At this time, the format of the encoded data is selected such that the DC components and the AC components are positively separated from each other in one synch block, for example, as shown in Fig. 2.

The respective separated data are then inputted to ECC decoding circuits 103, 104 for detection and correction of the error caused during transmission. The ECC decoding circuits 103, 104 deliver the corrected data to decoding circuits 105, 106 and, simultaneously, deliver error information to a DC replacement circuit 108 depending on the respective correction results.

The respective encoded data corresponding to the DC component and the AC component after the correction processing are inputted to the decoding circuits 105, 106 and then subjected to decoding processing for restoration into information of the DC component and the AC component. If any error still remains in the encoded data, the correct information cannot be of course restored.

In the case of using variable-length encoding, for example, as an encoding method for the AC component, it may happen that the decoded value of the AC component does not become a true value and, besides, even the number of data is not restored.

The respective decoded data outputted from the decoding circuits 105, 106 are transformed by an inverse orthogonal transform circuit 107 from values indicating the frequency components into data indicating a pixel value in the block. However, if the error cannot be completely corrected by the ECC decoding circuits 103, 104 as mentioned before, the input value to the inverse orthogonal transform circuit 107 is not in itself correct information and thus an output value of the inverse orthogonal transform circuit 107 will be data quite different from the correct pixel data.

Therefore, when the error information produced from the ECC decoding circuit 103 indicates that no error is present in the DC components for the relevant block, and the error information produced from the ECC decoding circuit

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104 indicates that the uncorrectable error is present in the AC components for the relevant block, a DC replacement circuit 108 replaces all the pixel values in the relevant block by the respective values given by the DC components.

With the above replacing operation, even if the correction impossible error still remains as mentioned above, each pixel value in the block is given by the value of the DC component which is representative of an average value, meaning that the data can be restored to a value, though not exactly the same as the true value, relatively close to the true value.

The respective data are rearranged by a time base transform circuit 109 to line up on the same time base as for the video signal inputted to the encoding device, followed by delivery from an output terminal 110. The output terminal 110 is connected to a monitor, printer or the like for forming an image.

According to the image decoding device thus arranged, even if the uncorrectable error occurs on the transmission path, a deterioration of image quality is minimized.

(Second Embodiment)

Fig. 3 shows a second embodiment of the present invention.

In the second embodiment of Fig. 3, the function effected by the DC replacement circuit 108 in Fig. 1 is realized by a 0 replacement circuit 308. The other circuit blocks are the same as those in Fig. 1 and, therefore, are denoted by the same reference numerals.

When the respective error information outputted from the ECC decoding circuits 103, 104 indicate that no error is present in the DC components for the relevant block and the uncorrectable error is present in the AC components for the relevant block, as with the above first embodiment, the 0 replacement circuit 308 replaces all the values of the AC components. With that replacing operation, the respective data inputted to the inverse orthogonal transform circuit 107 have their AC components set equal to 0. Consequently, the inverse orthogonal transform circuit 107 outputs the transformed data such that all the pixel values in the relevant block are given by the respective values of the DC component, with the result of the similar advantage to the foregoing first embodiment.

(Third Embodiment)

Fig. 4 shows an example indicating the fact that the present invent ion is also applicable to a different method of arranging the error detecting and correcting codes.

In this embodiment, the ECC decoding circuit 104 in the decoding device of Fig. 1 and the ECC encoding circuit 411 in the encoding device of Fig. 1 are located upstream of the separation circuit 102 and downstream of the synthesis circuit 412, respectively, as an ECC decoding circuit 304 and an ECC encoding circuit 311. The error detecting and correcting codes are formed for the data resulted from synthesizing the DC component and the AC component.

In this case, the error information outputted from the ECC decoding circuit 304 indicates that an error is present in the transmitted data, and the error information outputted from the ECC decoding circuit 103 indicates that no error is present in the DC components, this means that replacement of the AC component by the DC component is effective. Thus, the replacement can be performed by the same DC replacement circuit 108 as that in Fig. 1.

According to the above first to third embodiment of the present invention, as described above, by using means for detecting and correcting an error caused during transmission or in reproduction from a recording medium, and means for replacing all the decoded data in the relevant block by respective values given by DC components based on error information produced from the detecting and correcting means, or other means identical to the latter means, it is possible to minimize a deterioration of image quality even if an uncorrectable error occurs, and also realize an image decoding device which requires the small amount of hardware to be added.

Especially, in the above embodiments, a frequency transform coefficient due to the orthogonal transform is encoded using the DC component and the AC component in separate fashion. Therefore, when an error in the AC component cannot be corrected, the DC component can be used for error correction.

According to the above embodiment of the present invention, deterioration of an image quality of the image decoding device can be reduced.

(Fourth Embodiment)

An image processing apparatus according to a fourth embodiment of the present invention, described below, includes means for generating error detected information when a predetermined dynamic range of conversion coefficients is exceeded, and means for correcting the data falsely decoded, therey solving the problem as set forth above.

Fig. 6 is a block diagram showing this embodiment.

In Fig. 6, image data applied to an input terminal 41 is delivered to a discrete cosine transform (referred to as a DCT) unit 43 and subjected to a two-dimensional DCT for each block of 8 x 8 pixels. In this case, for example, it is supposed that a transform coefficient of 12 bits is obtained for image data of 8 bits.

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After performing the two-dimensional DCT, the transform coefficient is linearly quantized by a quantizer 45. The quantization step size is different for each transform coefficient. The quantization step sizes for the respective transform coefficients are given as values resulted by multiplying quantization coefficients generated from a quantization matrix unit 49 and shown in Table 2 below, for example, by 2^S. Here, S is called a scaling factor and outputted to not only a multiplier 47 but also a multiplexer 61. The multiplier 47 multiplies an output of the quantization matrix unit 49 by 2^S and delivers the resulting coefficient to the quantizer 45. Thus, image quality and the number of data generated are controlled depending on a value of S. Specifically, with the scaling factor S increasing, the amount of data is reduced but image quality deteriorates. With the scaling factor S decreasing, the amount of data is enlarged but image quality ameliorates.

Table 2

16	11	10	16	24	40	51	61
12	12	14	19	26	58	60	55
14	13	16	24	40	57	69	56
14	17	22	29	51	87	80	62
18	22	37	56	68	109	103	77
24	35	55	64	81	104	113	92
49	64	78	87	103	121	120	101
72	92	95	98	112	100	103	99

As regards to a DC component of the orthogonal transform coefficient quantized by the quantizer 45, a one-dimensional forecaster 53 makes forecast and a resulting forecast error is Huffman-encoded by a Huffman encoder 55 and then outputted to the multiplexer 61. The Huffman encoder 55 divides outputs of the forecast errors into 16 groups as shown in Table 3 below, for example. The identification (ID) number SSSS of the group to which the forecast error belongs is first Huffman-encoded and then expressed by an equi-length code indicating any value in the relevant group. In the case of Table 3, the code length of the equi-length code is equal to the value of the group ID number SSSS.

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Table 3

Forecast Error of DC Transform after Quantization	Group ID Number SSSS
0	0
- 1,1	1
- 3,-2,2,3	2
- 7 ~ - 4,4 ~ 7	3
- 15 ~ - 8,8 ~ 15	4
- 31 ~ - 16,16 ~ 31	5
- 65 ~ - 32,32 ~ 65	6
- 127 ~ - 64,64 ~ 127	7
- 255 ~ - 128,128 ~ 255	8
- 511 ~ - 256,256 ~ 511	9
- 1023 ~ - 512,512 ~ 1023	10
- 2047 ~ - 1024,1024 ~ 2047	11
- 4095 ~ - 2048,2048 ~ 4095	12
- 8191 ~ - 4096,4096 ~ 8191	13
- 16383 ~ - 8192,8192 ~ 16383	14
- 32767 ~ -16384,16384~ 32767	15

As for an AC component of the orthogonal transform coefficient except for the DC component, the output of the quantizer 45 is outputted to a zig-zag scanner 57. The zig-zag scanner 57 performs zig-zag scan from a low-frequency component to a high-frequency component as shown in Fig. 7. Thereafter, an output of the zig-zag scanner 57 is delivered to a Huffman encoder 59.

The Huffman encoder 59 divides the transform coefficients, which have the quantization results other than 0 (hereinafter referred to as significant coefficients), into 15 groups depending on their values and sets the group ID number as SSSS, as shown in Table 4 below. The number of the transform coefficients, which are sandwiched between the preceding and succeeding significant coefficients and have the quantization results equal to 0 (hereinafter referred to as insignificant coefficients), is set as a run length NNNN. Then, the group ID number SSSS and the run length NNNN are combined into a set, as shown in Table 5, followed by the Huffman encoding. Subsequently, the ID number SSSS is expressed by an equi-length code indicating any value in the relevant group shown in Table 4.

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Table 4

Quantization Output Level of AC Orthogonal Transform Coeff.	Group ID Number SSSS
- 1,1	1
- 3,-2,2,3	2
- 7 ~ - 4,4 ~ 7	3
- 15 ~ - 8,8 ~ 15	4
- 31 ~ - 16,16 ~ 31	5
- 65 ~ - 32,32 ~ 65	6
- 127 ~ - 64,64 ~ 127	7
- 255 ~ - 128,128 ~ 255	8
- 511 ~ - 256,256 ~ 511	9
- 1023 ~ - 512,512 ~ 1023	10
- 2047 ~ - 1024,1024 ~ 2047	11
- 4095 ~ - 2048,2048 ~ 4095	12
- 8191 ~ - 4096,4096 ~ 8191	13
- 16383 ~ - 8192,8192 ~ 16383	14
- 32767 ~ - 16384,16384~ 32767	15

In the case of Table 4, the code length of the equi-length code is equal to the value of the group ID number SSSS. The case that the value of the run length NNNN exceeds 16 is dealt with by sending a code of R16 shown in Table 5 and repeatedly subtracting 15 from the run length NNNN until the remainder becomes equal to or less than 15. When all the significant coefficients in the block are completely encoded, a code of EOB (End of Block) in Table 5 is finally sent.

Table 5

Group ID Number SSSS			
		0	1 2 ..... 14 15
Run Length NNNN	0	EOB	Huffman code for combination of NNNN and SSSS
	1	no use	
	2		
	.		
	.		
	.		
	.		
	14		
	15	R16	

The multiplexer 61 multiplexes the Huffmanencoded data of the DC component and the Huffman-encoded data of the AC component, followed by delivery to an output terminal 63 after adding the scaling factor S thereto.

Fig. 5 shows a block diagram a decoding device in cooperation with the encoding device of Fig. 4.

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The transmitted data is inputted to an XO terminal 11 and delivered to a divider 13. The divider 13 outputs the scaling factor S to a multiplier 29, the DC component data to a Huffman decoder 15, and the AC component data to a Huffman decoder 19. The Huffman decoder 15 decodes a series of Huffman codes to difference values and then outputs them to a difference decoder 17. The difference decoder 17 restores each difference value to the transform coefficient of the DC component and then outputs it to a terminal a of a switch 23.

On the other hand, the Huffman-encoded data of the AC component is restored by the Huffman decoder 19 to the transform coefficient of the AC component. After that, the restored transform coefficient is reverted by a scan recovery unit 21 from the zig-zag scan series to a data series as shown in Fig. 8, followed by delivery to a terminal b of the switch 23. Thus, both the transform coefficients of the DC component and the AC component are multiplexed as shown in Fig. 8 through the switch 23.

The multiplexer 29 multiplies the matrix produced from a quantization matrix unit 27 by 2^{-S} and outputs the resulting products to an inverse quantizer 25. The transform coefficients of 8 x 8 are inversely quantized by the inverse quantizer 25 and outputted to an inverse discrete cosine transform unit 31 for restoring to the image data of 8 bits.

While the transform coefficient inversely quantized by the inverse quantizer 25 is outputted to the inverse discrete cosine transform unit 31, it is also outputted to a judgment unit 37. The image data restored by the inverse discrete cosine transform unit 31 is outputted to not only a terminal a of a switch 39 but also a frame memory 35. The frame memory 35 delays the image data by a time period of one frame and then outputs the delayed data to a terminal b of the switch 39 for the purpose of using it as correction data when an error is detected.

The judgment unit 37 compares the transform coefficient with a predetermined dynamic range and outputs the judgment result to the switch 39.

Assuming now that the dynamic range of transform coefficients is 12-bit, for example, if the transform coefficient exceeds 12 bits, this leads to a judgment that an error has occurred in the transmission path. When the result of the judgment unit 37 judges the occurrence of an error, the switch 39 is changed over for connection to the terminal b so that the current image data is replaced by the image data at the same location of preceding one frame. When the judgment reveals the presence of no error, the switch 39 is changed over for connection to the terminal a. The image data whose error has been corrected through the switch 39 is delivered to an output terminal 33.

It is needless to say that although this embodiment makes a correction using a group of pixels of preceding one frame, the correction may performed by using other group of surrounding pixels which has high correlation. In this case, the frame memory 35 for storing the image data of preceding one frame can be dispensed with and, as a result, the circuit configuration is simplified.

Further, although the above judgment has been made by using the frequency component before transform into the actual space, the image data after being restored to the real space through the inverse DCT may be instead used.

The above judgment is performed for each pixel and, if an error is found in at least one component in the block, the entire block is replaced by the image data of the preceding frame. Alternatively plural blocks or an entirety of one picture may be replaced.

In addition, the orthogonal transform is not limited to the DCT and may be any other suitable one such as an Hadamard transform.

In place of Huffman encoding, other multi-value data encoding, arithmetic encoding or the like may also be used.

With this embodiment thus arranged, since there are provided error detecting means specific to the decoding process and error correcting means, image quality can be simply prevented from deteriorating when an error occurs.

As explained above, according to the fourth embodiment of the present invention, it is possible to prevent a deterioration of image quality otherwise caused by the occurrence of an error, and reproduce good image quality.

(Fifth Embodiment)

Fig. 9 illustrates a block diagram showing a configuration of a fifth embodiment of the present invention. Denoted at 210 is an input terminal for an analog image signal, 212 is an A/D converter for converting the analog image signal into a digital image signal, 214 is an encoder for encoding the digital image signal with high efficiency, and 216 is an ECC (error detecting and correcting code) addition circuit for adding an ECC so as to detect and correct a transmission error which may be caused in a recording/reproducing system such as a magnetic tape or optical disk, a commumication/transmission system such as an optical fiber or communication satellite, etc. 218 is a transmission path which is practically in the form of a recording/reproducing system such as a magnetic tape or optical disk, or a communication/transmission system such as an optical fiber or communication satellite.

Denoted at 220 is an ECC decoding circuit corresponding to the ECC addition circuit 216, and 222 is a decoder corresponding to the encoder 214. The ECC decoding circuit 220 outputs the error corrected data to the decoder 222 and outputs an uncorrectable error signal (flag) for the data including an error which cannot be corrected. uncorrectable error signal (flag) is delayed through frame memories 233, 235 by a time period of two frames and then supplied to a switch control circuit 236 described later. 224, 226, 228 are frame memories serially interconnected and each comprising an FIFO (first-in first-out) memory. 230 is a correlation detecting circuit for detecting correlation between an output

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of the decoder 222 and an output of the frame memory 224, i.e., interframe correlation, whereas 230 is a correlation detecting circuit for detecting interframe correlation between outputs of the frame memories 224 and 226. 234 is a switch for selecting any one of the outputs of the frame memories 224, 226, 228. Depending on the uncorrectable error flag from the ECC decoding circuit 220 and the detection results of the correlation detecting circuits 230, 232, the switch control circuit 236 changes over the switch 234. 238 is a D/A converter for converting the data selected by the switch 234 into an analog signal, and 240 is an output terminal for the reproduced analog image signal.

Fig. 10 shows an exemplified circuit configuration of each of the correlation detecting circuit 230, 232. 242, 244 are input terminals for respective image data, and 246 is a subtracter for calculating the difference between the two image data applied from the input terminals 242, 244. 248 is an adder and 250 is a D flip-flop for feeding an output of the adder 248 back to the adder 248 while delaying it by a time period of one sample. The adder 248 and the D flip-flop 250 cooperate to constitute an accumulator. An output of the adder 248 resulted from adding the current output of the subtracter 246 and the preceding one-frame output thereof is delivered from an output terminal 252.

Operation of this embodiment shown in Fig. 9 will now be described. The A/D converter 212 samples the analog image signal, applied to the input terminal 210, at a predetermined sampling rate for converting it into a digital signal of 8 bits or 16 bits. The encoder 214 compresses the digital image signal outputted from the A/D converter 212, namely, encodes the digital image signal with high efficiency through DPCM encoding or ADCT encoding. This embodiment is not restricted by the type of high-efficient encoding itself. The ECC addition circuit 216 adds the error detecting and correcting code in accordance with a predetermined method.

The output of the ECC addition circuit 216 is inputted to the ECC decoding circuit 220 via the transmission path 218 in the form of a recording/reproducing system or communication/transmission system. During transmission through the transmission path 218, there occurs a transmission error at certain probability. The ECC decoding circuit 220 checks the data inputted from the transmission path 218 for detecting the presence or absence of an error, the position of the error, and whether the error can be corrected or not, followed by delivery to the decoder 222 after correcting the correction possible error. When the correction impossible error is found, the error correction impossibe flag is outputted to the switch control circuit 236.

The decoder 222 decodes (expands) the data compressed by the encoder 214 and outputs the original image data to both the frame memory 224 and the correlation detecting circuit 230. Since the frame memories 224, 226, 228 are operated in an FIFO manner and cascaded to each other, the image data of successive three frames are sequentially stored in the frame memories 224, 226, 228. The correlation detecting circuit 230 detects correlation between the current frame (the output of the decoder 222) and the frame preceding one (the output of the frame memory 224), whereas the correlation detecting circuit 232 detects correlation between the frame preceding one (the output of the frame memory 224) and the frame preceding twos (the output of the frame memory 226) with respect to the current frame (the output of the decoder 222). The correlation detecting circuits 230, 232 each store one frame of differences between the corresponding image signals of two frames inputted thereto, and determines a degree of correlation between the two frames.

The switch 234 can select any one of the outputs from the frame memories 224, 226, 228 and normally selects the output of the frame memory 226. The switch control circuit 236 can find the position of the correction impossible error over the picture based on the error correction impossible flag from the ECC decoding circuit 220, and also find which one of the preceding picture and the succeeding picture has a higher degree of correlation with respect to the output picture of the frame memory 226, based on the outputs from the correlation detecting circuits 230, 232. Stated otherwise, in response to the error correction impossible flag from the ECC decoding circuit 220, the switch control circuit 236 changes over the switch 234 to thereby select the image data at the same position on the picture which has a higher degree of correlation.

The D/A converter 238 converts the image data outputted from the switch 234 into an analog signal, following which the reproduced analog image signal is outputted from the output terminal 240.

(Sixth Embodiment)

Fig. 11 illustrates a block diagram showing a configuration of a sixth embodiment of the present invention. This embodiment adopts an ADCT method as a high-efficient encoding method.

Denoted at 1110 is an input terminal for an analog image signal, 1112 is an A/D converter, and 1114 is an encoder of ADCT type. The encoder 1114 separates the input data into a DC component and an AC component through a DCT transform made for each DCT block, e.g., 8 x 8 pixels, performs DPCM encoding on the DC component between the current DCT block and the preceding DCT block, and simultaneously performs run-length processing and Huffman encoding on the AC component. 1116 is an ECC (error detecting and correcting code) addition circuit for adding an ECC to the respective encoded outputs of the AC component and the DC component from the ADCT encoder 1114.

1118 is a transmission path or system, 1120 is an ECC decoding circuit corresponding to the ECC addition circuit 1116, and 1122 is an ADCT decoder corresponding to the ADCT encoder 1114. 1124, 1126, 1128 are frame memories serially interconnected and each comprising an FIFO (first-in first-out) memory. 1129, 1130 are frame memories of

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FIFO type for delaying the DC component outputted from the ADCT decoder 1122 by a time period of one frame, and are cascaded for detecting correlation. 1131 is a correlation detecting circuit for detecting interframe correlation between an output of the decoder 1122 and an output of a frame memory 1129, whereas 1132 is a correlation detecting circuit for detecting interframe correlation between outputs of the frame memories 1129 and 1130. 1134 is a switch for selecting any one of the outputs of the frame memories 1124, 1126, 1128. Depending on the error correction impossible flag from the ECC decoding circuit 1120 and the detection results of the correlation detecting circuits 1131, 1132, a switch control circuit 1136 changes over the switch 1134. 1138 is a D/A converter for converting the data selected by the switch 1134 into an analog signal, and 1140 is an output terminal for the reproduced analog image signal.

Specific operation of this embodiment shown in Fig. 11 will now be described. The A/D converter 1112 converts the analog image signal, applied to the input terminal 1110, into a digital signal. The ADCT encoder 1114 carries out a DCT transform on the digital image signal outputted from the A/D converter 1112 for each DCT block such that the DC component is subjected to DPCM encoding between the current DCT block and the preceding DCT block, and the AC component is subjected to run-length processing and Huffman encoding. The ECC addition circuit 1116 adds an ECC to the AC component output and the DC component output from the ADCT encoder 1114.

The output of the ECC addition circuit 1116 is inputted to the ECC decoding circuit 1120 via the transmission path 1118. The ECC decoding circuit 1120 checks the respective AC and DC component data inputted from the transmission path 1118 for detecting the presence or absence of an error, the position of the error, and whether the error can be corrected or not, followed by delivery to the ADCT decoder 1122 after correcting the correction possible error. When the correction impossible error is found, an error correction impossible flag is delayed through frame memories 1133, 1135 by a time period of two frames and then supplied to the switch control circuit 1136.

The ADCT decoder 1122 performs DPCM decoding on the DC component and both Huffman decoding and run-length decoding on the AC component, followed by an inverse DCT transform for restoring to the original image data. The image data restored by the ADCT decoder 1122 is applied to the frame memory 1124, whereas the DC component before the inverse DCT transform is applied to both the frame memory 1129 and the correlation detecting circuit 1131 for the DC component. As with the frame memories 224, 226, 228 in Fig. 10, the frame memories 1124, 1126, 1128 respectively store the image data of successive three frames in a sequential manner. The frame memories 1129, 1130 are also cascaded to store the DC components of adjacent two frames on a frame-by-frame basis. As for the DC component, the correlation detecting circuit 1131 detects correlation between the current frame (the output of the decoder 1122) and the frame preceding one (the output of the frame memory 1129), whereas the correlation detecting circuit 1132 detects correlation between the frame preceding one (the output of the frame memory 1129) and the frame preceding twos (the output of the frame memory 1130) with respect to the current frame. The correlation detecting circuits 1131, 1132 may be the same circuit configuration as that shown in Fig. 10, and each store one frame of differences in the DC component between the corresponding image signals of two frames inputted thereto. Thus, a degree of correlation between the two frames can be determined.

The switch 1134 can select any one of the outputs from the frame memories 1124, 1126, 1128 and normally selects the output of the frame memory 1126. The switch control circuit 1136 controls the switch 1134 in a like manner to the switch control circuit 236 shown in Fig. 9. Specifically, for the error correction impossible data, the switch control circuit 1136 enables to select the image data at the same position on the picture which has a higher degree of correlation. The D/A converter 1138 converts the image data outputted from the switch 1134 into an analog signal, following which the reproduced analog image signal is outputted from the output terminal 1140.

With this embodiment shown in Fig. 11, since correlation is detected by using the DC component, correlation detection can be performed more correctly and, therefore, interpolation can be performed in a more natural manner.

While the illustrated embodiment include the correlation detecting circuits disposed on the decoder side (or the reception side), those circuits may be disposed on the encoder side (or the transmission side) so as to transmit information of interframe correlation frame by frame. This remarkably cut down the equipment burden to be borne on the reception side. Accordingly, this modification is fit for such a transmission system that is directed to a large number of receivers like TV broadcasting and requires the small size and reduced cost of receiver units.

According to the fifth and sixth embodiments, as will be easily understood from the above description, since information of interframe correlation is used to interpolate the error correction impossible data, it is possible to make the perforation in a more natural manner and provide a reproduced image (received image) with less unnaturalness.

(Seventh Embodiment)

Fig. 12 is a block diagram showing a seventh embodiment of the present invention. Transmitted data applied to an input terminal 631 is decoded by a run-length decoder 633 to a DPCM code, and the 0 run-length of the data is outputted from the run-length decoder 633 to a counter 632. The counter 632 continues counting both the 0 run-length and the number of DPCM codes until arrival of a reset synch bit. In other words, the counter 632 counts the predetermined number of pixels in a processing unit. The number of pixels counted by the counter 632 is outputted to a comparator 636. The comparator 632 compares the predetermined number of pixels set by a processing unit setter 634 and the

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number of pixels outputted from the counter 632, thereby outputting an error flag of 1 bit to a switch 640. Stated otherwise, if both the numbers of pixels are not in match with each other, then a flag is set based on judging the presence of an error.

Meanwhile, the DPCM code decoded by the run-length decoder 633 is outputted to the DPCM decoder 635 and further decoded to image data. The image data outputted from the DPCM decoder 635 is delivered to a delay unit 638. The delay unit 638 delays the image data by a predetermined amount of delay caused in the comparator 636, to thereby match the timing between the error flag and the image data. The image data outputted from the delay unit 638 is delivered to a contact a of the switch 640 and, simultaneously, to a one-line delay unit 639 so that the same image data is delivered to a contact b of the switch 640 after being delayed by a time period of one line. When the error flag outputted from the comparator 636 indicates that no error has occurred, the switch 640 is changed over for connection to the contact a. When an error has occurred, the switch 640 is changed over for connection to the contact b so that the current image data is replaced by the image data of preceding one line for correction. In either case, the correct or corrected image data is delivered to an output terminal 637.

It is needless to say that while the above embodiment is explained as using the encoding method in combination of DPCM encoding and run-length encoding, this embodiment is applicable to all the methods that use run-length encoding, such as one in which run-length encoding is performed after orthogonal transform encoding. Also, the principles of this embodiment can be employed in any of the foregoing embodiments as well.

As described above, according to the seventh embodiment of the present invention, it is possible to prevent a deterioration of image quality otherwise caused by the occurrence of an error, by providing error detecting means specifically adapted for the process of decoding run-length codes.

(Eighth Embodiment)

Fig. 17 is a block diagram showing an encoding method which combines twos, i.e., the orthogonal transform encoding method and the run-length encoding method, with each other. Image data applied to an input terminal 711 is divided into blocks by a block formation unit 713 such that a raster series of Fig. 18A is turned into a plurality of blocks as shown in Fig. 18B. In this case, each block comprises 8 pixels horizontal and 8 pixels vertical. The pixel data in each block are transformed by a transform encoder 715. The transform encoder 715 employs a transform encoding method called a discrete cosine transform (DCT) encoding.

Generally, as shown in Fig. 19, the coefficients obtained through the DCT transform of the image data exhibit low resolution in the oblique direction and has the smaller magnitude at the higher frequency component. Those coefficients obtained through the DCT transform are quantized by a quantizer 717. The quantized transform coefficients are scanned by a zig-zag scanner 717 in zig-zag fashion as shown in Fig. 20 for the reason that the probability of the occurrence of 0 is increased at the higher frequency component. Such zig-zag scan results in successive appearance of 0s. The zig-zag scanned data is applied to a run-length encoder 721 to form a set of the number of 0s and the coefficients other than 0. Upon the completion of processing of one block, an EOB code is outputted. An entropy encoder 723 assigns a short code to those codes having high occurrence probability and a long code to those codes having low occurrence probability, followed by delivery to a transmission format unit 725. The transmission format unit 725 delivers the data from an output terminal 727 after adding a synch bit for every several blocks as shown in Fig. 21.

Fig. 16 is a block diagram showing a configuration of a decoding device in cooperation with the encoding device of Fig. 17. The data transmitted through a transmission path is applied to an input terminal 731 and decoded by an entropy decoder 733 to a run-length code.

The run-length decoder 751 performs run-length decoding and outputs the decoded data to an inverse zig-zag scanner 737 and, simultaneously, outputs the sum of the number of 0s in a run and the number of 1s other than 0, i.e., the number of transform coefficients, to a counter 753. The counter 753 counts the number of transform coefficients for each predetermined period of time. Assuming now that the predetermined period of time is one block, a processing unit setter 755 sets 64 equal to the number of transform coefficients. A comparator 757 compares a value inputted from the processing unit setter 755 with a value inputted from the counter 753. If both the values are in match with each other, then it is judged that the data has been transmitted without errors. If both the values are not in match with each other, then it is judged that an error has occurred. Either judgment result is outputted to a delay unit 759. The delay unit 759 delays the judgment result by the amount to be paid off by proceeding through an inverse zig-zag scanner 737, an inverse quantizer 739 and an inverse transform encoder 741.

On the other hand, the inverse transform encoder 741 outputs the inversely transformed pixel data to one terminal a of a switch 763 and also to a frame memory 761. The frame memory 761 the pixel data, which are delayed by a time period of one frame therethrough, to the other terminal b of the switch 763. Depending on the judgment result outputted from the delay unit 759, the switch 763 selects the terminal a for a predetermined period of time when no error is found, and the terminal b for a predetermined period of time when an error is found. In other words, upon the occurrence of an error, the current image data is replaced by the image data of preceding frame for correction.

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A raster formation unit 743 converts the block series back into the raster series, followed by delivery to an output terminal 743.

As described above, according to the eighth embodiment of the present invention, a deterioration of image quality otherwise caused by the occurrence of an error can be prevented with a simple hardware construction, by providing error detecting means specifically adapted for the process of run-length decoding.

It should be understood that the uncorrectable error in the foregoing embodiments may be performed by using any of the image data of preceding frame and the image data of preceding field.

Furthermore, the present invention is not limited to the foregoing embodiments and can be variously modified and applied within a scope defined by the attached claims.

Additionally, any combinations of the foregoing embodiments are covered by the principles of the present invention.

Claims

1. An image processing apparatus comprising:

receiving means (731) for receiving an image signal including encoded orthogonal transform coefficients;
decoding means (733-741, 751) for decoding the encoded orthogonal transform coefficients on a two-dimensional pixel block unit basis, and for converting the orthogonal transform coefficients into pixel-representative image data;
detection means (751-759) for detecting transmission errors of the encoded orthogonal transform coefficients; and
concealment means (761, 763), responsive to said detection means (751-759), for concealing transmission errors by outputting pixel-representative image data for the corresponding pixel block of the preceding field or frame in place of that for the current field or frame;

characterised in that:
said decoding means (733-741, 751) includes a run-length decoding means (751) for decoding received run-length encoded orthogonal transform coefficients; and
said detection means (751-759) includes counting means (753), responsive to said run-length decoding means (751), to count the number of orthogonal transform coefficients, inclusive of those of 0-value included in each decoded run, for a predetermined number of block or blocks, and comparator means (757) for comparing the count with a count of predetermined set value determined for the predetermined number of block or blocks.

2. An apparatus according to claim 1 wherein said decoding means (733-741, 751) is adapted to decode discrete cosine transform coefficients.

3. An apparatus according to any preceding claim wherein said decoding means (733-741, 751) is adapted to decode the encoded orthogonal transform coefficients on an NxN pixel block unit basis, where N is the number of pixels in each row and in each column of each block.

4. An apparatus according to any preceding claim wherein said detection means (751-759) is adapted to detect transmission errors by reference to parity check codes included in the image signal.

5. An apparatus according to claim 4 wherein said detection means (751-759) is adapted to detect transmission errors by reference to parity check codes included in the image signal for orthogonal transmission coefficients representing AC components, and for orthogonal transmission coefficients representing DC components, of the image represented by the image signal.

6. An image processing system comprising in combination:
transmitting means (401; 301) for transmitting an image signal including run-length encoded orthogonal transform coefficients, encoded on a two-dimensional pixel block unit basis; and
an image processing apparatus (402; 302) as claimed in any preceding claim 1 to 5.

7. A method of image processing comprising steps of:

receiving an image signal including encoded orthogonal transform coefficients;
decoding the received image signal on a two-dimensional pixel block unit basis and converting the orthogonal transform coefficients into pixel representative image data;
detecting transmission errors of the encoded orthogonal transform coefficients; and

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concealing the transmission errors, by outputting pixel representative image data for the corresponding pixel block of the preceding field or frame in place of that for a current field or frame;

characterised in that:

the received image signal includes run-length encoded orthogonal transform coefficients and said step of decoding includes run-length decoding; and

said step of detecting transmission errors includes counting the number of orthogonal transform coefficients, inclusive of those of 0-value included in each decoded run, for a predetermined number of block or blocks, and comparing the count obtained with a count of predetermined set value determined for the predetermined number of block or blocks.

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FIG. 1

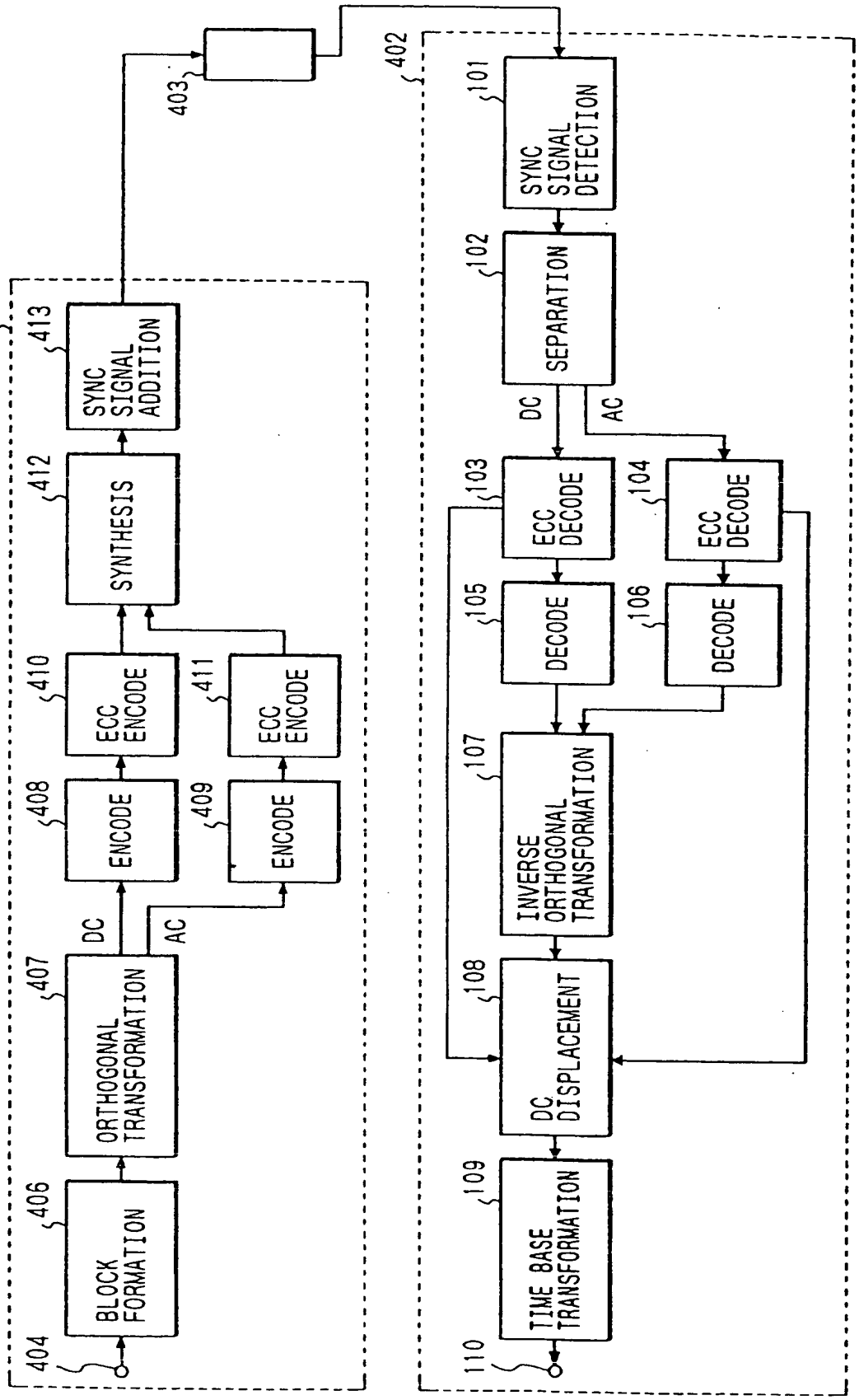

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FIG. 2

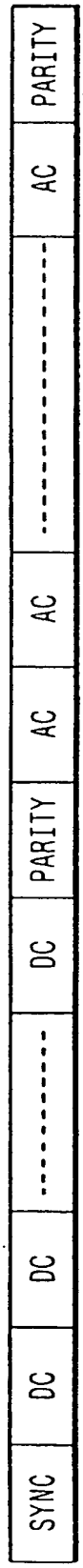

FIG. 3

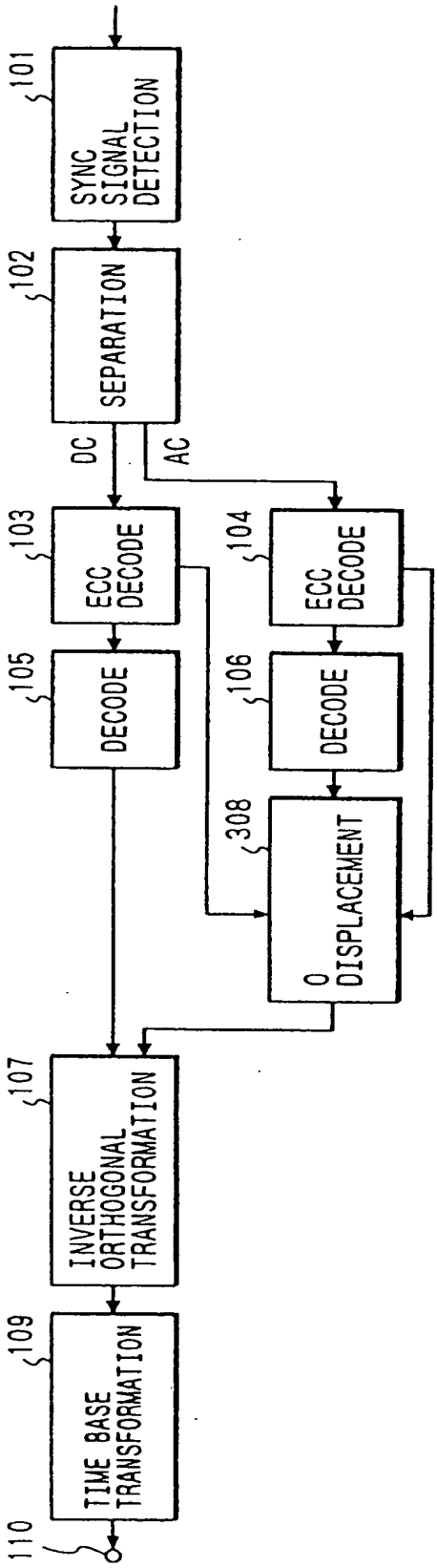

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FIG. 4

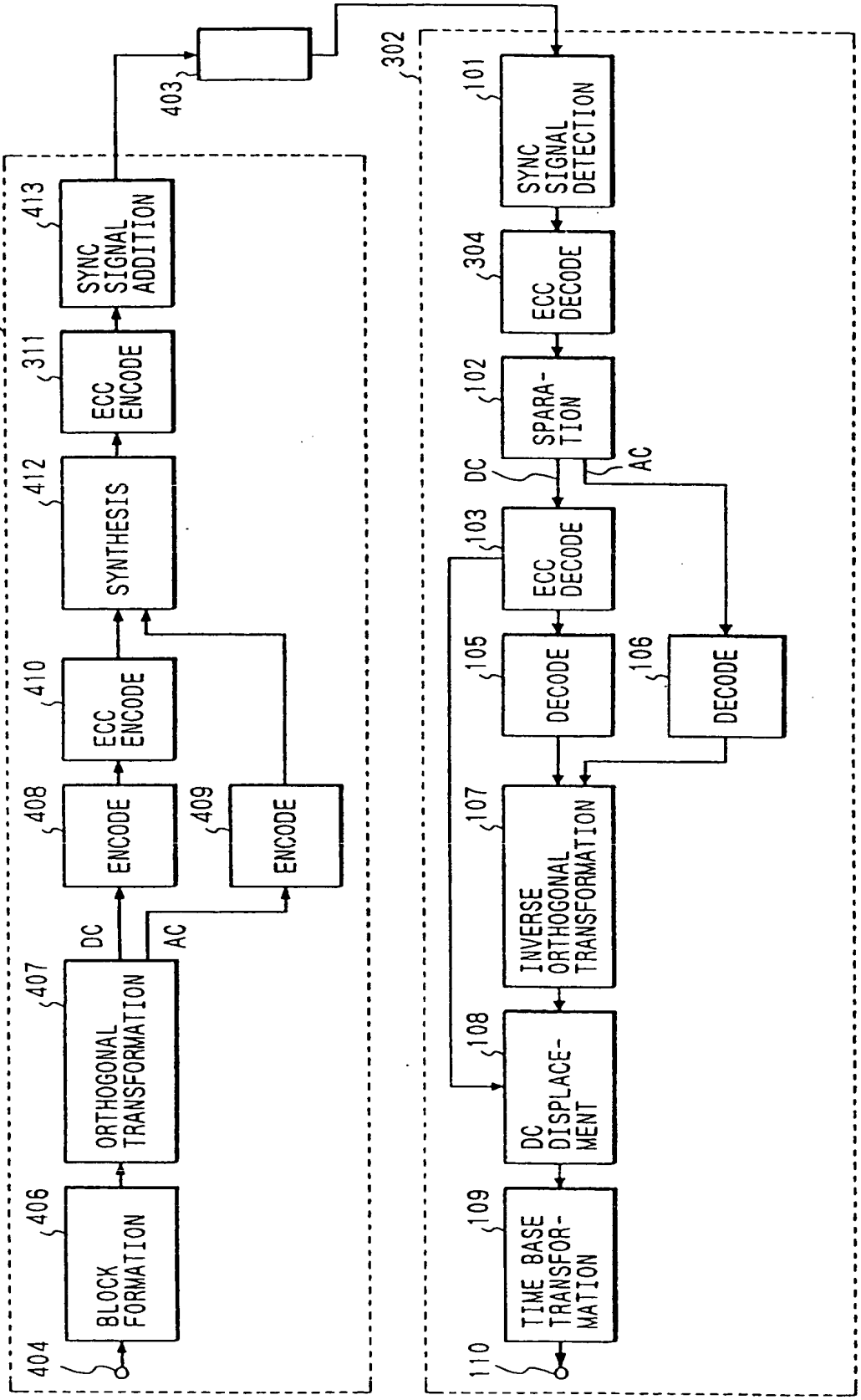

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FIG. 5

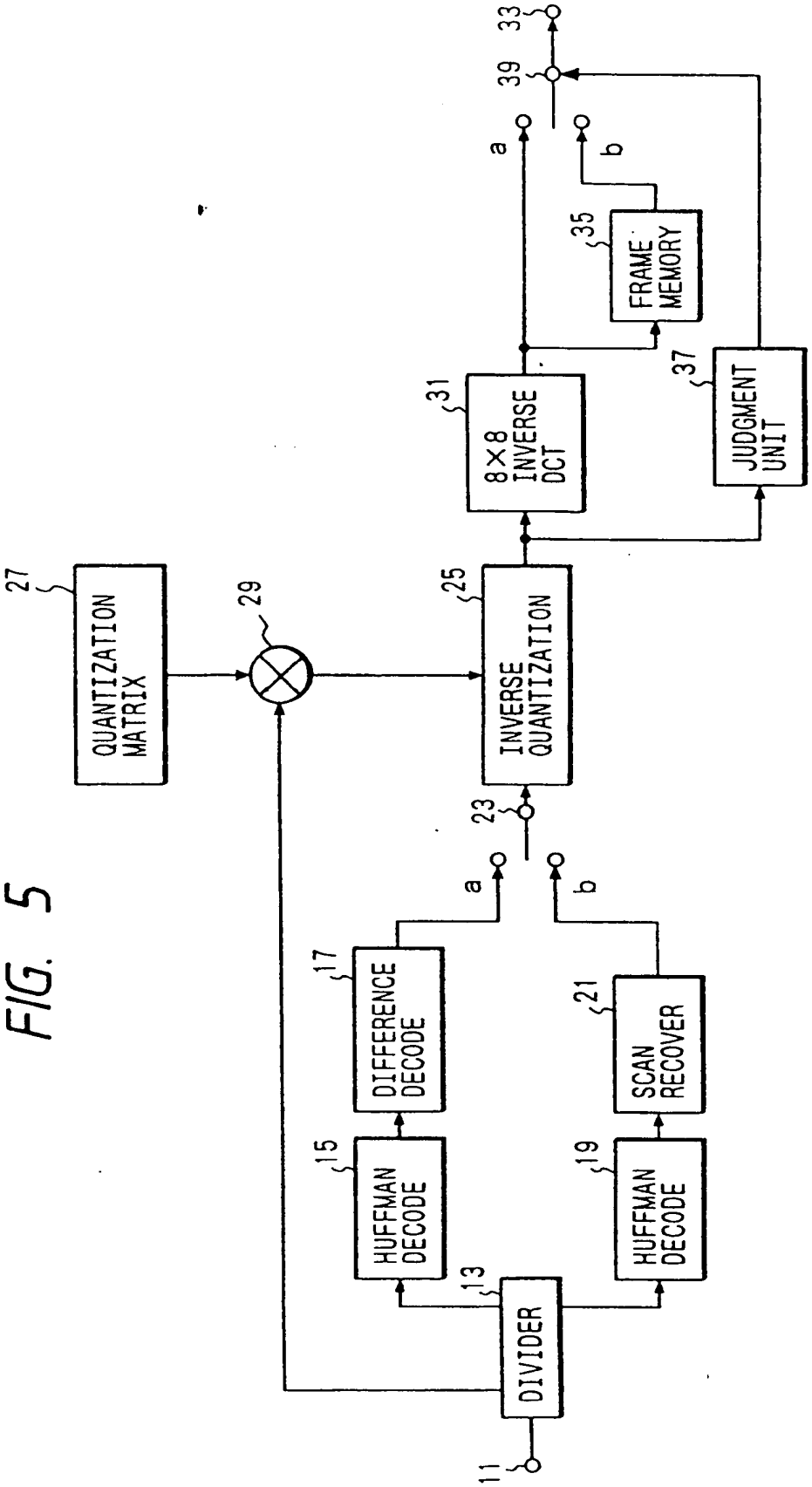

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FIG. 6

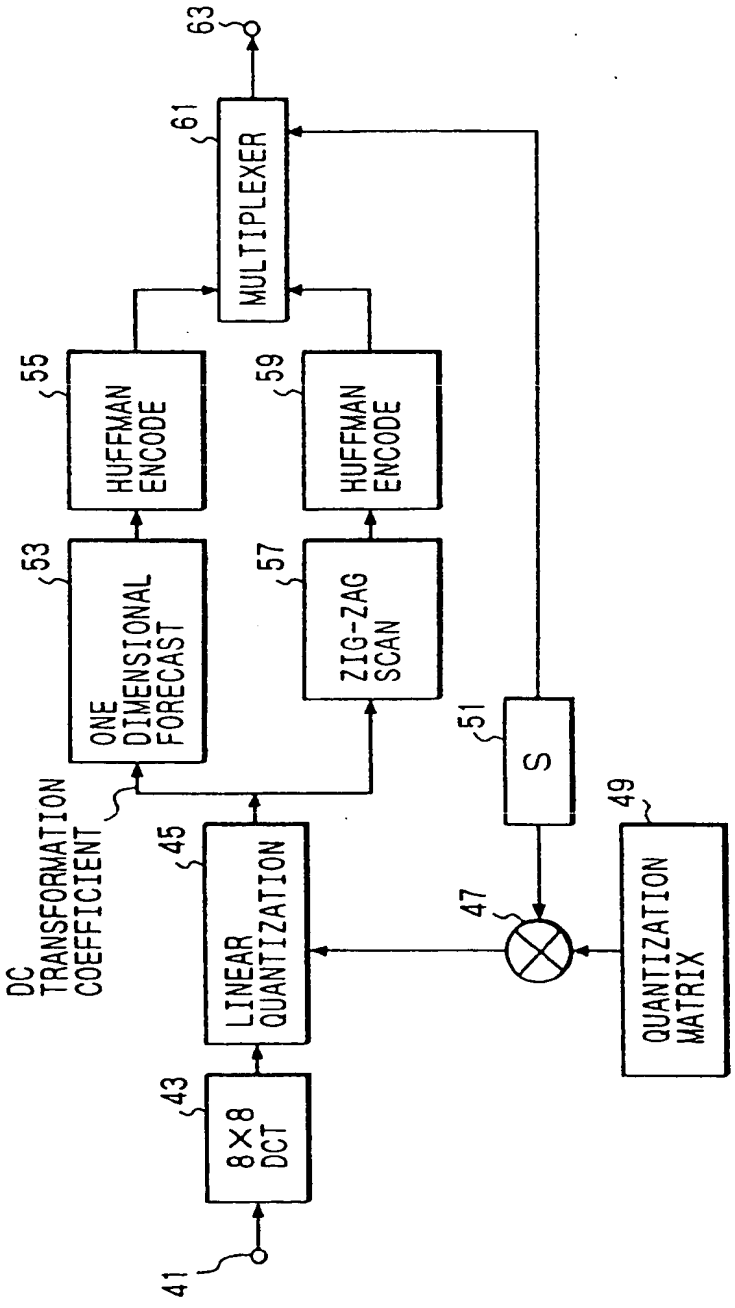

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FIG. 7

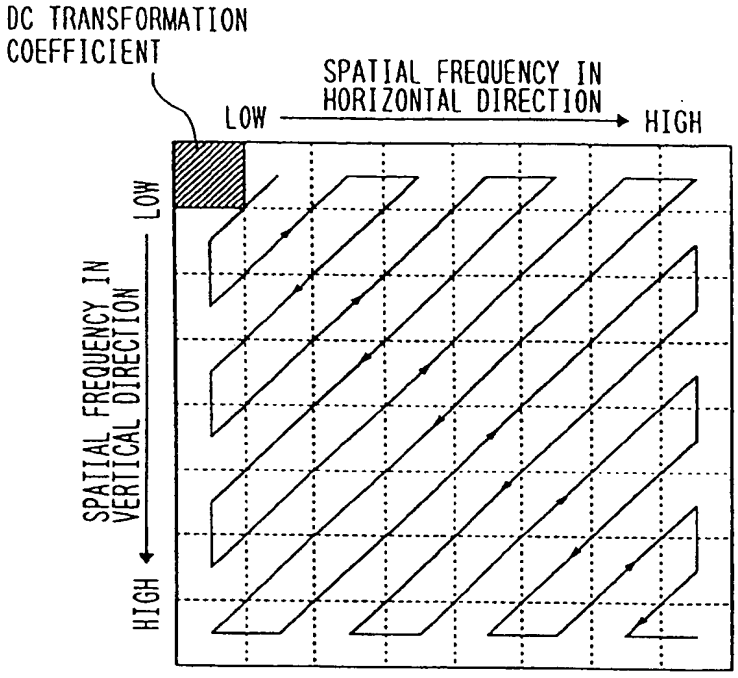
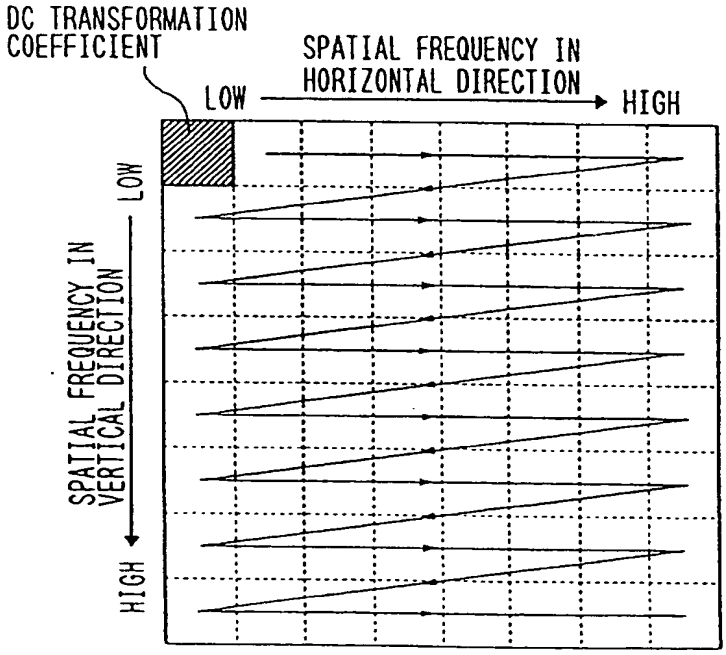


FIG. 8



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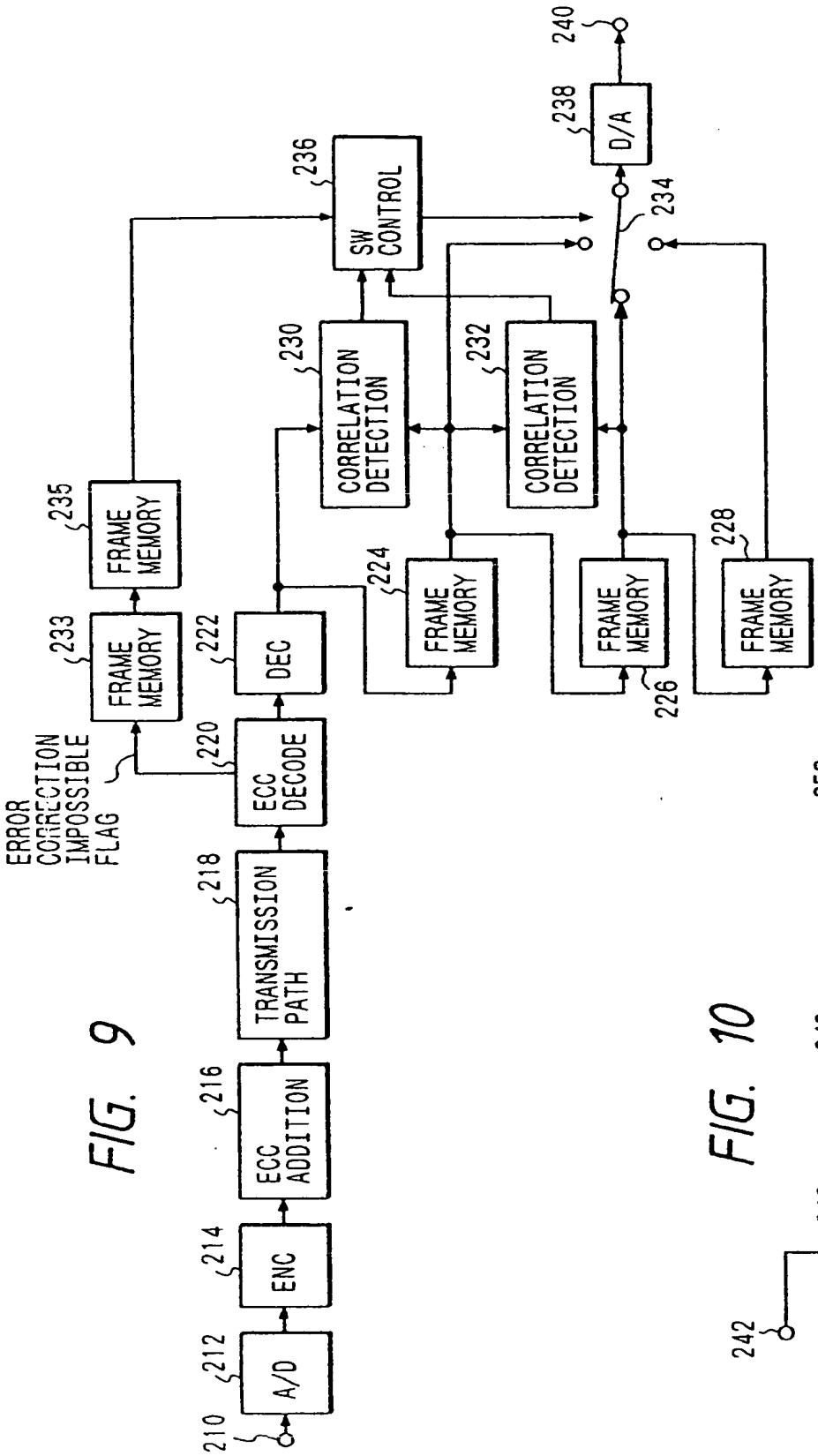

FIG. 9

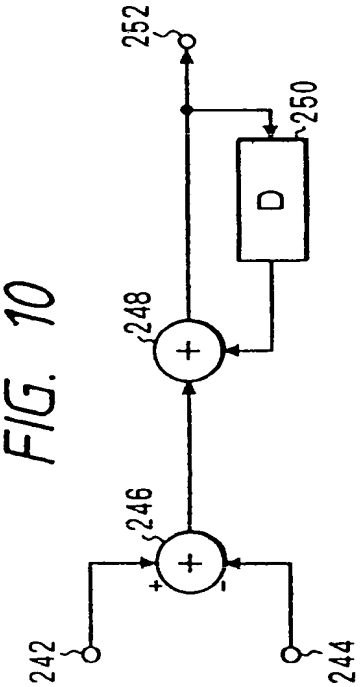

FIG. 10

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FIG. 11

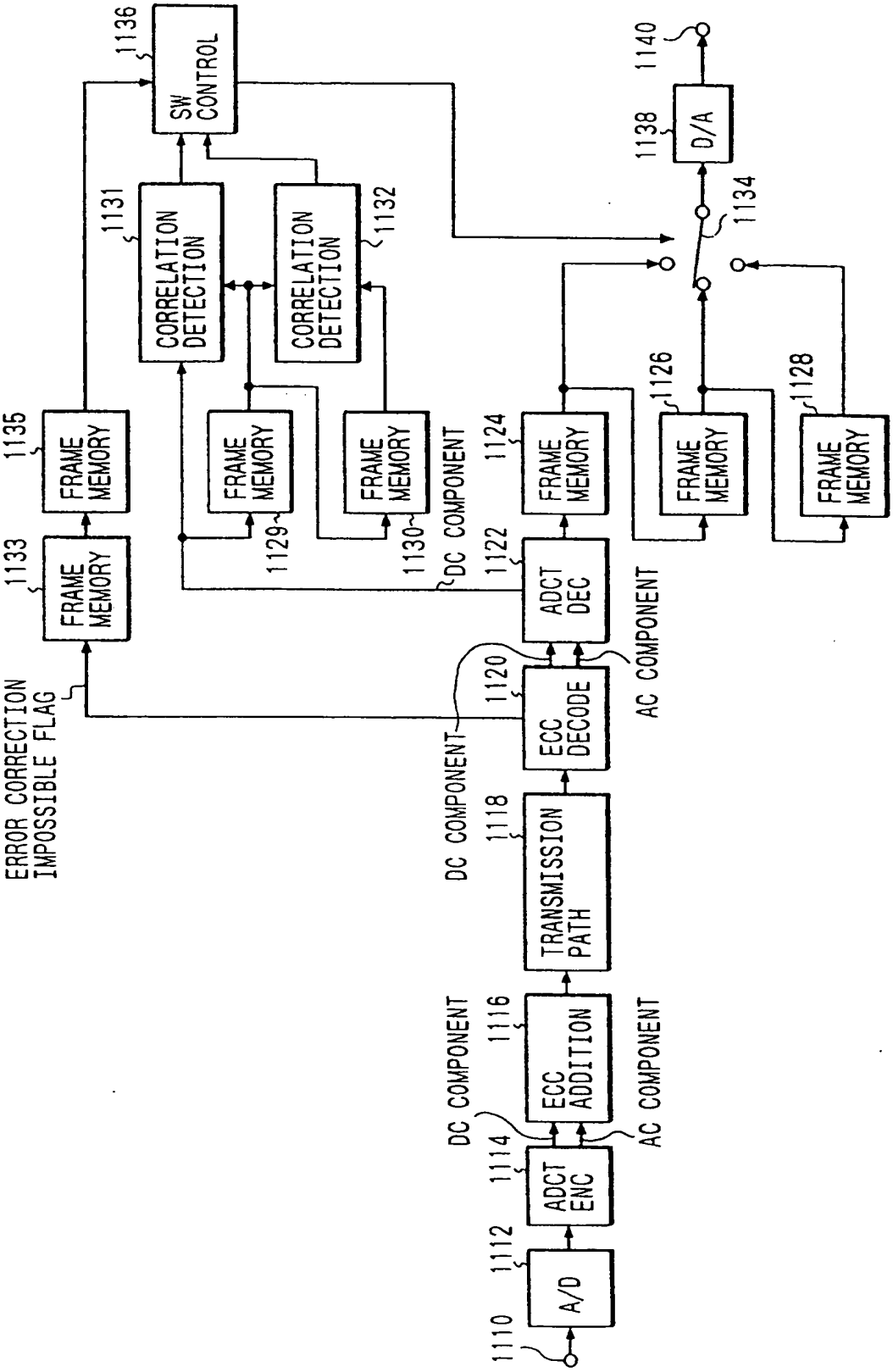

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FIG. 12

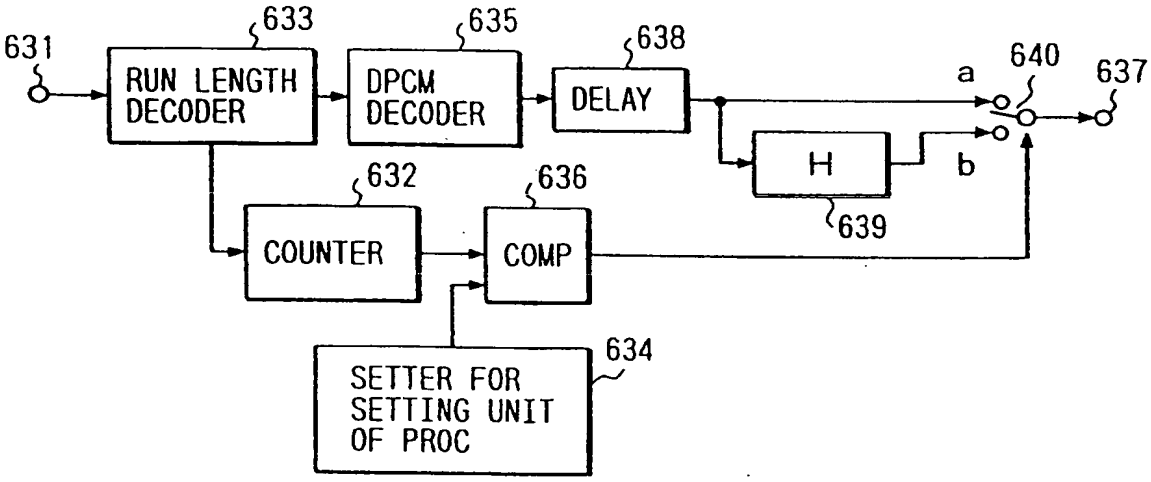

FIG. 13

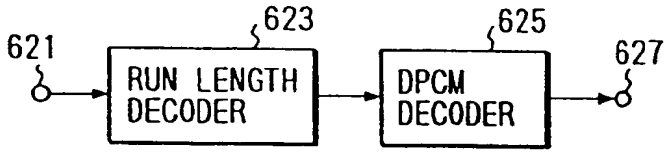

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FIG. 14

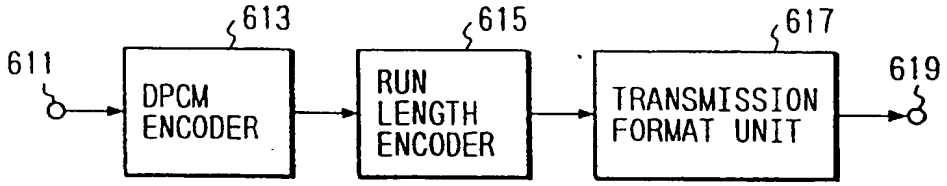


FIG. 15A

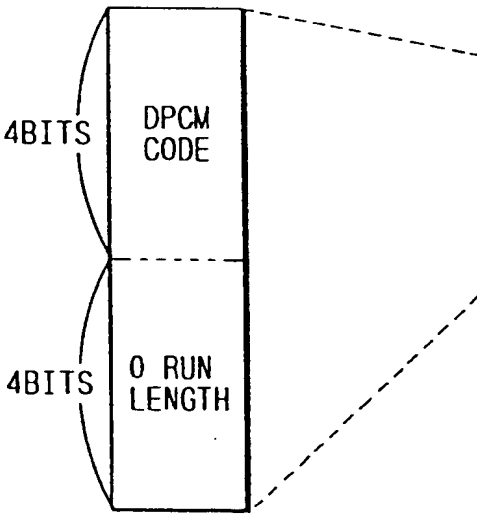
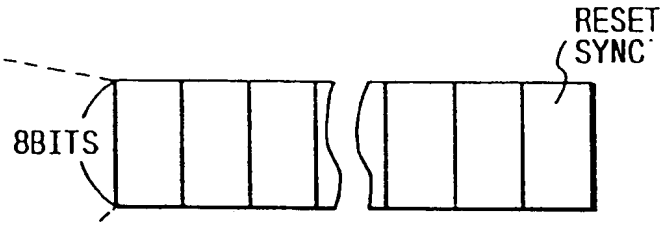


FIG. 15B



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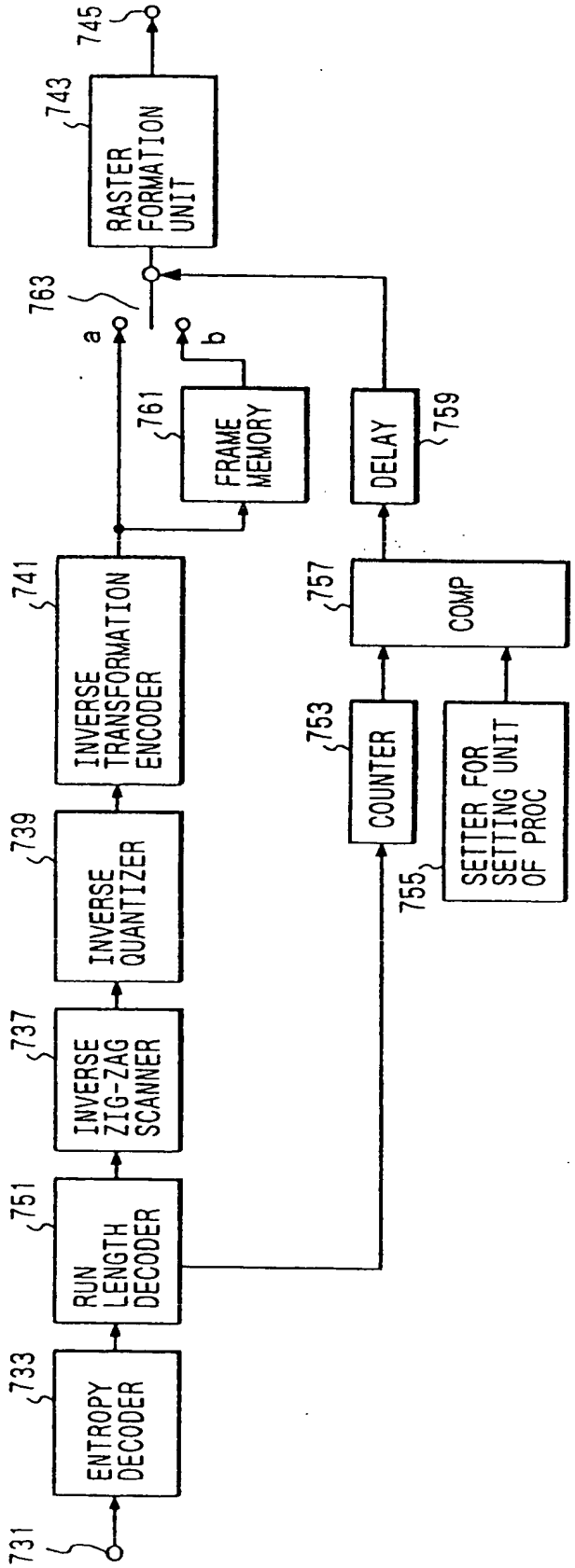

FIG. 16

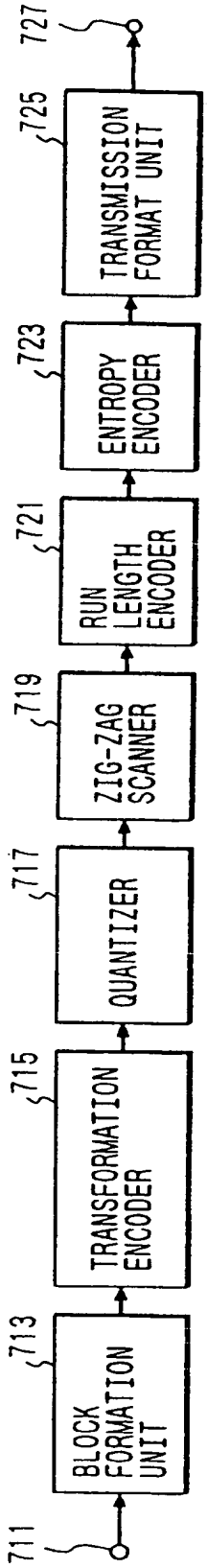

FIG. 17

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FIG. 18B

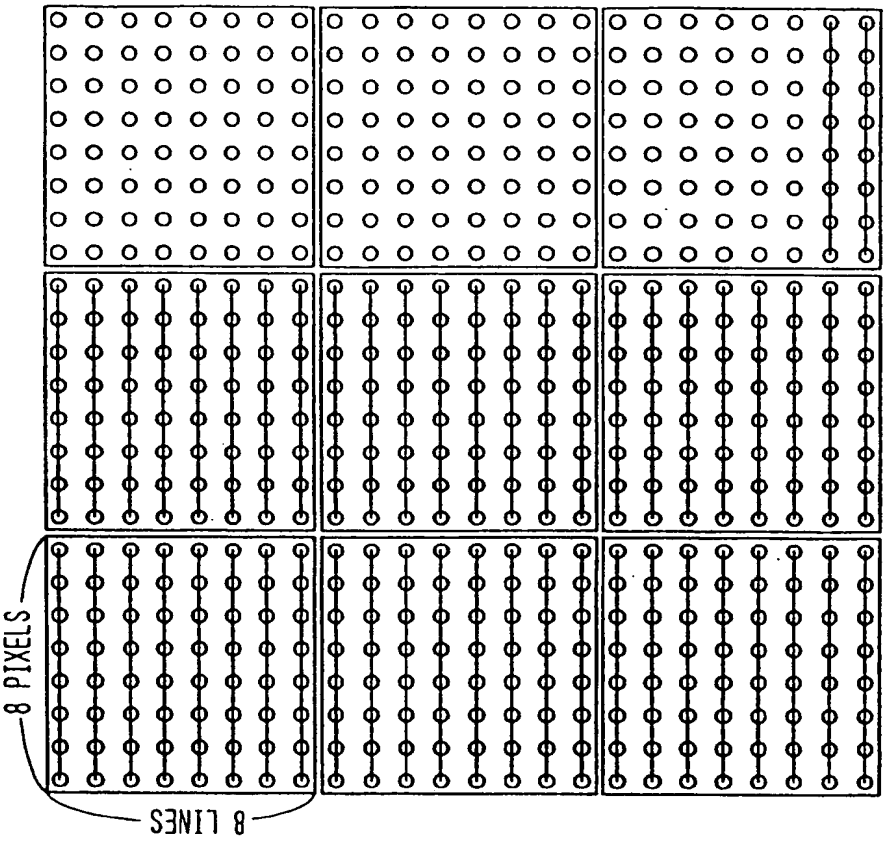

FIG. 18A

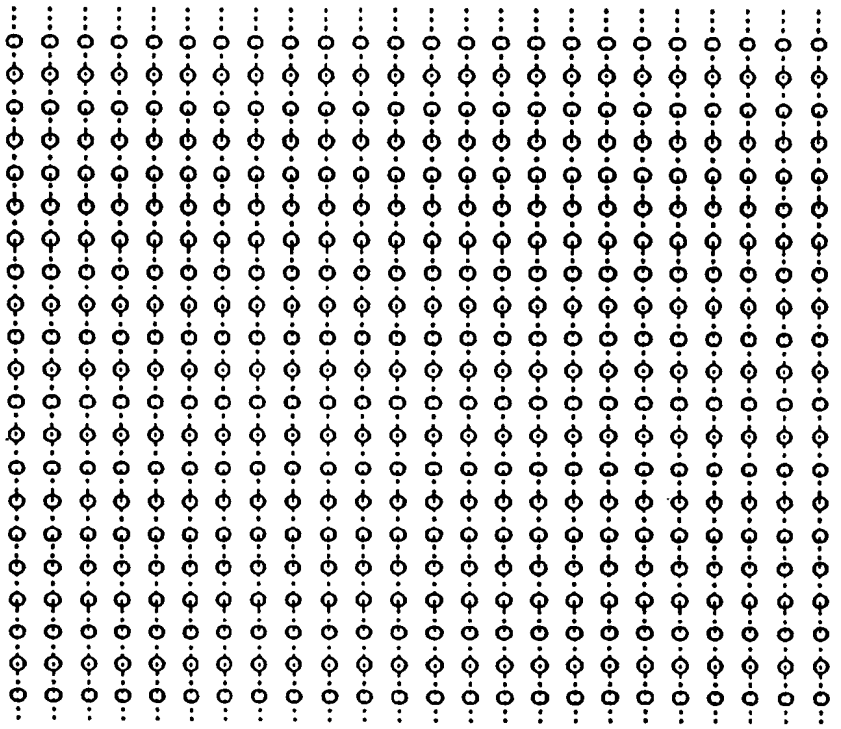

FIG. 19

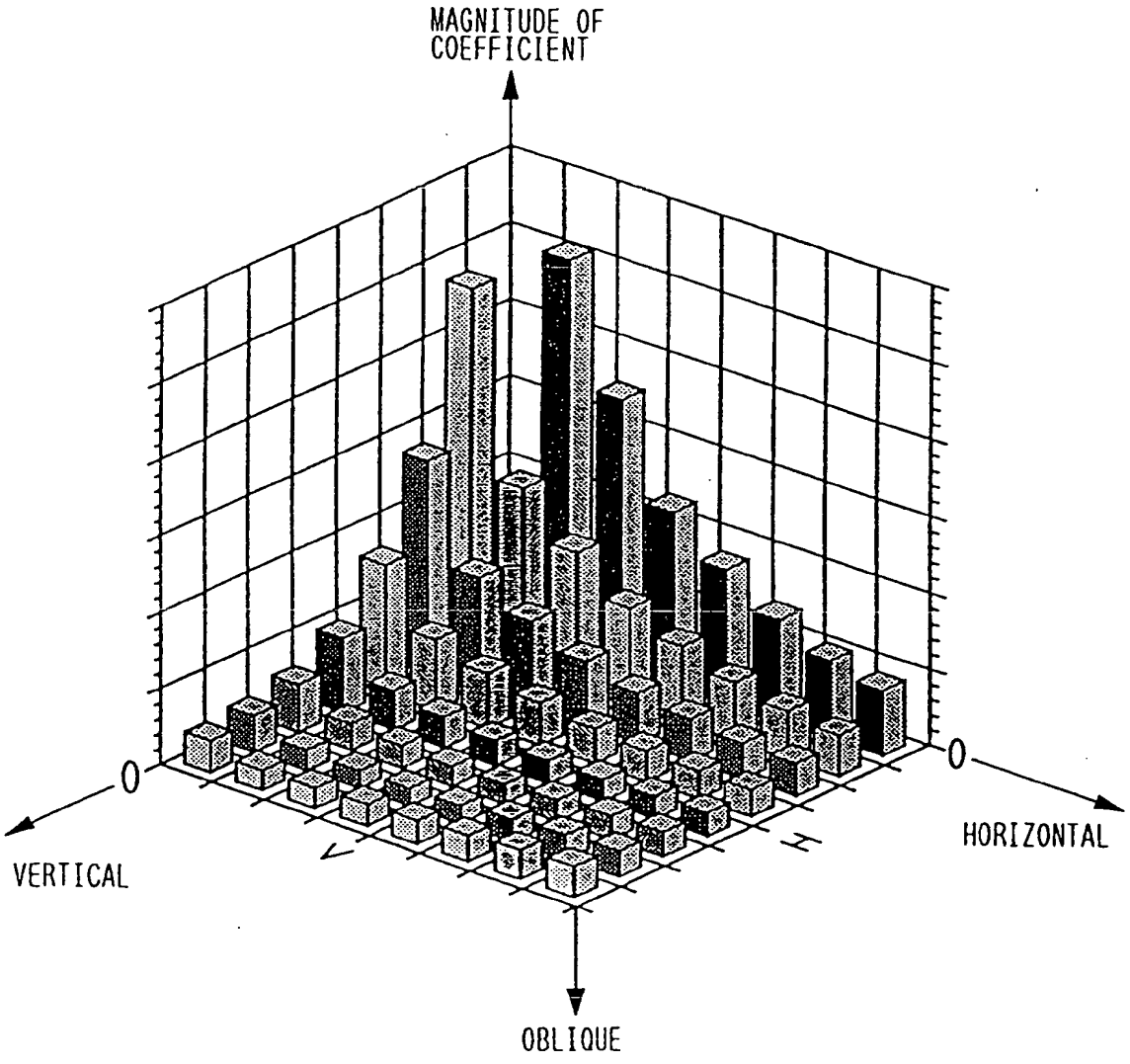

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FIG. 20

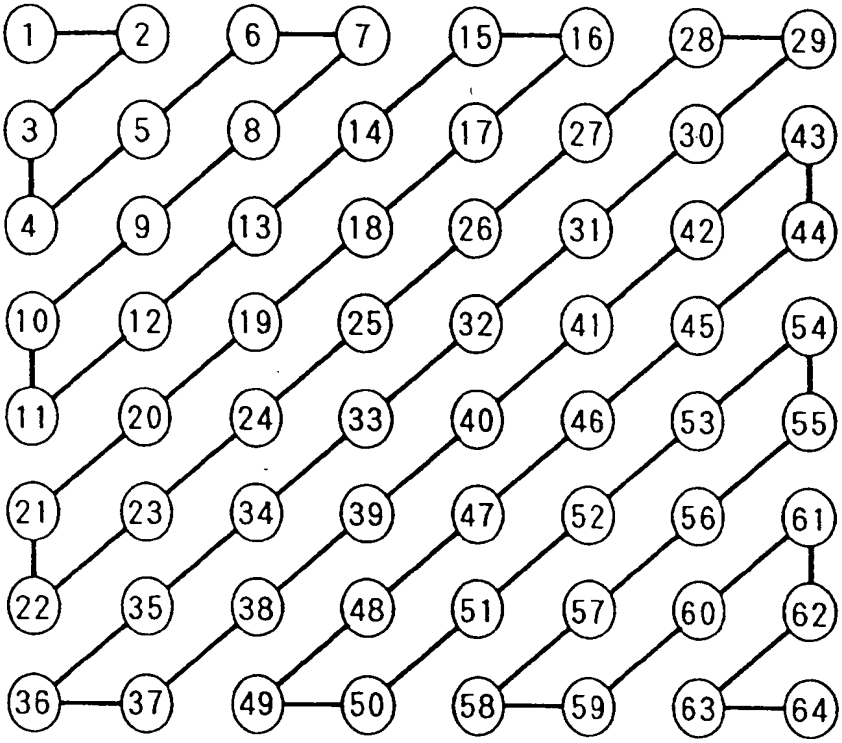

FIG. 21

SYNC	DATA
SYNC	DATA
SYNC	DATA
SYNC	DATA
SYNC	DATA
SYNC	DATA
SYNC	DATA

(19) Europäisches Patentamt
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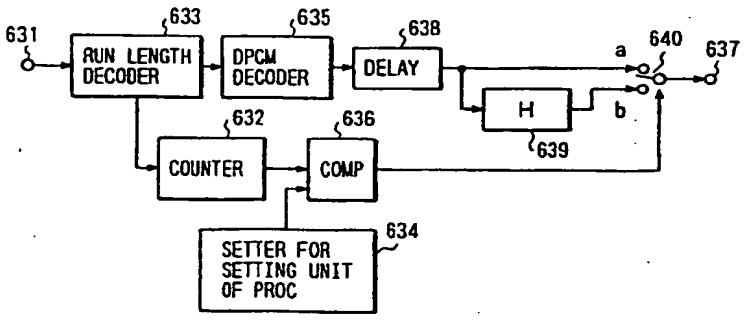
(54) Image processing apparatus

(57) An image processing apparatus and method in which an image signal including run-length encoded orthogonal transform coefficients is decoded and transmission errors in the coefficients are concealed by outputting substitute pixel data. Transmission errors are detected by counting the number of orthogonal transform coefficients, inclusive of those of 0-value included in each run, for a predetermined number of pixel block or blocks and by comparing the count obtained with a preset count.

FIG. 12



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Application Number
EP 96 20 2230

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	BARBERO M ET AL: "CODING STRATEGIES BASED ON DCT FOR THE TRANSMISSION OF HDTV" SIGNAL PROCESSING OF HDTV, L'AQUILA, FEB. 29 - MAR. 2, 1988, no. WORKSHOP 2, 29 February 1988, CHIARIGLIONE L, pages 503-508, XP000075087 * paragraph 2 * ---	1-7	H04N7/30 H04N7/64
A	US 4 903 269 A (FEDELE NICOLA J) * abstract; figure 3 * ---	1-7	
A	US 4 189 748 A (REIS JAMES J) * abstract; figures 1,8 * ---	1-7	
A	US 4 807 033 A (KEESEN WERNER ET AL) * abstract * * column 1, line 38 - line 50 * -----	1-7	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 December 1997	Berbain, F

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